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Appl. No. 10/661,793  
Appeal Brief dated 02/18/2009Attorney Docket No.: TS01-1037  
N1085-90149

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chi-An Kao et al.

Examiner: Khiem D. Nguyen

Serial No.: 10/661,793

Group Art Unit: 2823

Filed: 09/12/2003

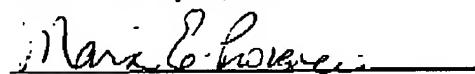
Confirmation No.: 8353

For: CONSTANT AND REDUCIBLE HOLE BOTTOM CD IN VARIABLE POST-CMP  
THICKNESS AND AFTER-DEVELOPMENT-INSPECTION CD

## CERTIFICATE OF MAILING/FACSIMILE TRANSMISSION PURSUANT TO 37 C.F.R. §1.8

I hereby certify that this correspondence (and anything referred to as being transmitted herewith) is being facsimile transmitted to the United States Patent and Trademark Office (Fax No. 571-273-8300) on the date shown below.

Date: February 18, 2009

  
 Marla E. Provencio

Examiner Khiem D. Nguyen  
 Mail Stop Appeal Brief - Patents  
 Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, VA 22313-1450

APPEAL BRIEF – 37 CFR § 41.37

Commissioner:

This is an appeal from the Final Rejection of claims in the above-identified application, as made in the final Office action dated July 2, 2008 and the Advisory Action mailed September 24, 2008.

This filing is further to the Pre-Appeal Brief Request for Review filed October 31, 2008 and responsive to the Notice of Panel Decision from Pre-Appeal Brief Review mailed December 18, 2008.

Enclosed is the fee for filing an Appeal Brief under 37 CFR § 41.20(b)(2) in the amount of \$540.00. This Appeal Brief is being filed in accordance with 37 CFR § 41.37,

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PAGE 6/24 \* RCVD AT 2/18/2009 6:58:03 PM [Eastern Standard Time] \* SVR:USPTO-EFXRF-6/29 \* DNIS:2738300 \* CSID:6197442201 \* DURATION (mm:ss):08:54

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and is timely filed with a One Month Extension of Time and the appropriate fee, in accordance with 37 CFR § 1.136 and based on the December 18, 2008 mailing date of the Notice of Panel Decision from Pre-Appeal Brief Review.

#### **1. REAL PARTY IN INTEREST**

The real party in interest is Taiwan Semiconductor Manufacturing Company, Ltd. The rights to this application were originally assigned to Taiwan Semiconductor Manufacturing Company, Ltd., and that assignment recorded at Reel 014502/Frame 0019.

#### **2. RELATED APPEALS AND INTERFERENCES**

There are no related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal, that are known to Appellants or Appellants' attorney.

#### **3. STATUS OF CLAIMS**

Claims 8-17 are pending in this application with claims 8-11 and 15-17 having been rejected. Claims 12-14 were allowed. The rejection of each of claims 8-11 and 15-17 is hereby appealed.

#### **4. STATUS OF AMENDMENTS**

No amendments were filed after the final Office action of July 2, 2008. A response to the final Office action titled Response to Office Action Dated July 2, 2008 / Request for Reconsideration, was filed on August 29, 2008 and included Appellants' arguments, but did not include claim amendments. The Advisory Action dated September 29, 2008 actually indicates that the "proposed amendment(s) . . . will be entered", though no amendments were in fact filed.

Arguments were also presented in the Pre-Appeal Brief Request for Review filed October 31, 2008.

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## 5. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to the fabrication of integrated circuit devices and more particularly to methods for patterning etch resist material, i.e., photoresist and for forming openings in layers such as dielectric layers that underlie the etch resist material layer. The invention provides real-time feedback loops that dynamically control both the dimensions of the features formed in the etch resist material layer and the dimensions of the openings formed in the underlying layers.

The invention is described generally in the specification from page 5, line 1 through page 6, line 10 and also in the specification on page 7, line 5 through page 25.

Integrated circuits, also broadly referred to as semiconductor devices, are formed by producing a succession of material layers over a wafer or substrate and utilizing the material layers for various purposes. Many of the material layers are patterned and this generally occurs by forming a layer photoresist over the material layer, then forming an opening in the photoresist layer. The photoresist layer is used as an etch resistant "mask" layer and openings are formed in the subjacent layer using the mask layer, typically by etching. The openings formed in the subjacent material layer generally correspond to the openings in the pattern formed in the photoresist layer and include dimensions influenced by the dimensions of the corresponding opening formed in the patterned etch resist layer. It is of critical importance to control the dimensions of both the features, e.g., openings formed in the photoresist layer and similarly the features such as openings formed in the subjacent material layer. For each layer, measurements are made of the critical dimensions, such measurements commonly abbreviated as CD's. A photolithographic process followed by a develop process is used to pattern, i.e., form openings in, the photoresist layer: hence, the critical dimensions of the etch resist layer are referred to as "after develop inspect" ADI-CD's. The openings formed by etching in the underlying layer, are usually referred to as "after etch inspect" AEI-CD's, or "after clean inspect" ACI-CD's.

The invention provides for both monitoring and controlling the critical dimensions of the etch resist, i.e., photoresist, layer and also for monitoring and controlling the

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critical dimensions of openings formed in an underlying layer of insulation material, on a real-time basis.

Each of the independent claims recites, among other features, the feature of the control of the critical dimensions of the patterned layer of etch resist material. The invention provides for *controlling* the critical dimensions of the opening formed in the layer of etch resist material by *communicating* with the systems that actually produce the pattern in the photoresist layer and which are therefore responsible for the critical dimensions in the photoresist, i.e. etch resist, layer. Corrections are implemented via communication with the lithography tools, i.e. the means for creating an opening through a layer of etch resist material, to control the critical dimensions and assure that they are within specification values.

*The means, including the feedback mechanism, for assuring that the obtained critical dimension measurement of the opening created through the layer of etch resist material is within design specification<sup>1</sup>* as in claims 8, 15 and 16, is described in the specification, at least on page 12, line 18 through page 14, line 7 and on page 16, line 15 through page 17, line 12 and illustrated in FIG. 3A. FIG. 3A of the specification shows evaluation sub-system 42 communicating via software link/feedback line 44 to entry point 32 of the photoresist control function 30 which includes adjustment sub-system 34 that controls the critical dimension by providing corrections in the photo system. In particular, parameters of adjustment sub-system 34 are provided via software interface 35 to the process sub-system 36 (page 12, line 21 – page 13, line 2) which applies the data in order to create an opening through a layer of photoresist. This control and correction feature is further generally described at least on page 17, lines 7-13.

The means for creating an opening through a layer of etch resist material is shown as section 15 of FIG. 1 and photoresist function 30 of FIG. 3A. Section 15 is

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<sup>1</sup> Stated generally: see reproduced portions of claims 8, 15 and 16 in section 7B, *infra*, for exact claim language.

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described on page 8 which includes steps that comprise the means for creating an opening through a layer of etch resist material. Step 21, described on page 8, is a step of section 15 and is disclosed to be "*contact photo, which comprises:* • *depositing (coating) a layer of photoresist over the surface of the layer of insulation material* • *patternning and developing the layer of photoresist, creating an opening through the layer of photoresist, exposing the surface of the layer of insulating material where the hole has been created through this layer.* Since the means for creating an opening through a layer of etch resist material is disclosed to include depositing (coating), patterning and developing the layer of photoresist, such means inherently includes the coating system, the lithography system and the developer system hereinafter collectively referred to as "the lithography tools", as is also known and commonly referred to, by one of ordinary skill in the art.

The means for measuring an obtained critical dimension measurement of the opening created through the layer of etch resist material is recited at least as step 22 of section 15, also described on page 8 and shown in FIG. 1.

Photoresist control function 30, shown in FIG. 3A, includes adjustment sub-system 34 and also processes devices, i.e. forms openings in the layer of etch resist material, as evidenced by process sub-system 36 which precedes measurement sub-system 38 which measures the after develop CDs of the product produced at process sub-system 36. Process sub-system 36 is also described in the paragraph bridging pages 14-15 of the specification.

The means for creating an opening through a layer of insulation material are included in section 20 of FIG. 1, discussed on page 9 of the specification. Step 24 includes the actual etching of the hole through the layer of insulating material.

The means, including a feedback mechanism, for assuring that the opening created through the layer of insulation material is within design specification, are shown in FIG. 3B as etch control function 35 discussed beginning on page 18, line 16 of the specification.

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## 6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issue presented is whether the grounds of rejection stated by the Examiner in the July 2, 2008 Office action, are proper.

More particularly, the issue presented is whether or not the Examiner properly rejected claims 8-11 and 15-17 under 35 U.S.C. § 102(e) as being anticipated by Sahin, et al. (US Pub No. 2003/0220708 A1), hereinafter "Sahin."

## 7. ARGUMENT

### 7A. Final Rejection of Claims 8-11 and 15-17.

In the final Office action dated July 2, 2008, claims 8-11 and 15-17 were rejected under 35 U.S.C. § 102(e).

In particular, the Examiner rejected claims 8-11 and 15-17 under 35 U.S.C. Section 102(e) as being anticipated by Sahin, et al. (U.S. Patent Publication 2003/0220708), hereinafter "Sahin."

On August 29, 2008, Appellants filed a response to the final Office action of July 2, 2008. The August 29, 2008 response did not include claim amendments.

The Advisory Action issued September 24, 2008 maintained each of the rejections of the July 2, 2008 final Office action. The arguments in Appellants' Pre-Appeal Brief Request for Review filed October 31, 2008 address the rejections presented in the July 2, 2008 final Office action and which were maintained in the September 24, 2008 Advisory Action.

### 7B. Claims 8-11 and 15-17 are not subject to rejection under 35 U.S.C. Section 102(e) as being anticipated by Sahin.

The rejected independent claims are claims 8, 15 and 16. The claimed invention, as reflected in independent claims 8, 15 and 16, is distinguished from Sahin because the claimed invention uses a feedback mechanism to control the critical dimension

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measurement of the opening formed in the photoresist material by communication with the means for creating the opening through a layer of etch resist material, i.e., the coating, lithography and developing systems (collectively, "the lithography tools") that produce the openings in the photoresist material. This represents an in-process, real-time, dynamic correction of errors. In contrast, Sahin merely screens the wafers after openings are formed in the photoresist, measures the critical dimension measurement, determines if the wafer requires rework (if it is out of design specifications) and, if the wafer requires rework, directs the wafer to be reworked without doing anything to actually control the critical dimension measurement. Sahin does not communicate with, and makes no changes to, the lithography tools that would cause, much less assure, the reworked critical dimensions to be any different than the out-of-spec CD's that prompted the rework. Appellants respectfully submit that the mere designation of out-of-spec wafers for rework does not rise to the level of *controlling* the CDs by *communicating* with the lithography tools.

The claimed invention goes a step further than Sahin, as reflected in independent claims 8, 15 and 16.

In particular, independent claim 8 recites:

means, including a feedback mechanism, for assuring that the obtained critical dimension measurement ... is within design specification, said feedback mechanism communicating with said means for creating an opening through a layer of etch resist material to control said critical dimension measurement of said opening by implementing corrections in said means for creating an opening through a layer of etch resist material.

Independent claim 15 recites:

means, including a feedback mechanism, for obtaining a critical dimension measurement ... and assuring that said critical dimension measurement is within design specification, said feedback mechanism communicating with said means for creating an opening through a layer of etch resist material to control said critical dimension . . .

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Independent claim 16 recites:

means, including a feedback mechanism, for creating an opening through a layer of etch resist material ... such that the opening has a critical dimension measurement that is within design specification, said feedback mechanism communicating with said means for creating an opening through a layer of etch resist material to control said critical dimension measurement of said opening.

By communicating with the means for creating the opening, i.e., the lithography tools (as known to one in the art and as discussed, *supra*), the invention provides for controlling the CD in the etch resist layer, i.e., by influencing the lithography tools to produce a critical dimension that is within design specifications. Control is defined in Webster's II New College Dictionary, Houghton Mifflin Company, 1995 (copy attached hereto) as: **control**: *to exercise authority or influence over: direct.* As above, independent claim 8 recites that the feedback mechanism assures that the CD is within specification by communicating with the lithography tool to control the CD by implementing corrections in the means for creating an opening in the etch resist material, assuring that the CD produced by the lithography tools is within design specification. Claim 15 provides for assuring that the CD is within design specification using the feedback mechanism that communicates with the means for creating an opening through a layer of etch resist material to control the critical dimension and independent claim 16 provides the feedback mechanism communicating with the lithography tool to control the critical dimension of the opening (that extends through a layer of etch resist material).

For an anticipation rejection under 35 U.S.C. § 102, each of the claimed elements must be disclosed in a single prior art reference. According to the Federal Circuit, “[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration”, *W.L. Gore & Assoc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing *Soundscriber Corp. v. United States*, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). As such, Sahin does not

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anticipate the claims because Sahin fails to provide the claimed feature of controlling the critical dimension measurement by communicating with the means for creating an opening through a layer of etch resist material, i.e., (collectively) "the lithography tools".

The final Office action alleges, in the paragraph bridging pages 2-3, that Sahin discloses

*means, including a feedback mechanism (see page 12, paragraph [0166]), for assuring that the obtained critical dimension measurement of the opening created through the layer of etch resist material 708 is within design specification (see page 16, paragraph [0210] and step 809 in FIG. 8A(1)), the feedback mechanism communicating with the means for creating an opening through a layer of etch resist material 708 to control the critical dimension (CD) measurement of the opening 710a, 710b by implementing correction (see step 807) in the means for creating an opening through a layer of etch resist material (see page 6, paragraph [0211] and steps 807 and 810 of FIG. 8A(1)).*

Similarly, the subsequent Advisory Action states:

*it is respectfully submitted that Sahin does provide a feedback mechanism that communicates with the means for creating an opening of the photoresist material layer and control the critical dimension measurement of the opening by implementing corrections in the means for creating an opening.*

In support of this position stated in the Advisory Action, the Examiner refers to FIGS. 8A(1), 8A(2) and FIGS. 1A and 1B, as well as the corresponding portions of the specification, i.e., paragraphs [0064], [0070] - [0072], [0100] - [0105] and [0207] - [0212].

As a first matter, Appellants point out that paragraphs [0100] - [0105] of Sahin are directed to the etch system, not the lithography system.

With respect to the drawings and specification of Sahin that do address lithography, Sahin fails to anticipate the claimed features of communicating with the lithography tool, i.e., with the means for creating an opening through a layer of etch

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resist material. Sahin also fails to anticipate the claimed feature of communicating with the means for creating an opening through a layer of etch resist material to control the critical dimension measurement of the opening. Appellants point out that, in the excerpt from the final Office action reproduced above, the Examiner recites "the feedback mechanism communicating with the means for creating an opening through a layer of etch resist material 708". The Examiner provides no reference to the means for creating an opening nor the communication. Reference number 708 merely refers to the etch resist material shown in cross section in FIG. 7, not the means for creating an opening, i.e. the lithography tools, as above. The Examiner has not identified such a feature because Sahin does not provide such a feature.

Referring to the previously cited definition of control, the Sahin reference exercises no authority or influence over the critical dimension of the photoresist layer. Sahin merely determines that wafers that are out of specification should be reworked and provides for reworking the wafers without a) communicating with the lithography tools that are used to subsequently form the openings in the layer of etch resist material or b) controlling the critical dimension measurement of the opening.

Addressing the Examiner's cited paragraphs of Sahin, Appellants point out that paragraph [0064] of Sahin describes FIG. 1A which is a schematic diagram of system 100 for forming shallow trench isolation regions in a substrate. It is noteworthy to point out that module controller 114 and fab controller 116 are in apparent communication with a multitude of tools, i.e., etch tool 102, cleaning tool 104, oxidation tool 106, deposition tool 108, and planarization tool 110, with the conspicuous absence of a lithography tool. As such, Sahin clearly does not provide a feedback mechanism or any communication between the module controller and the means for creating an opening through a layer of etch resist material, i.e., the (collective) lithography tools, as in the claimed invention. Moreover, paragraph [0209] of Sahin provides: *the module controller 114 may reject the wafer (step 806) and the module controller 114 may direct the inventive system 100 to rework the wafer if possible (step 807). For example, if the wafer has a patterned masking layer formed with photoresist, the etch tool 102 may be employed to ash the photoresist layer and the cleaning tool 104 may be employed to*

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*remove any residual photoresist as previously described. The wafer may then be reprocessed via a lithography tool (not shown). The lithography tool itself, then, is outside of the purview of the inventive system 100. The lithography tool is not illustrated. No description of any communication with a lithography system is provided. The aforementioned paragraphs certainly do not disclose communicating with the lithography system.*

FIG. 8A(1), heavily relied upon by the Examiner, illustrates the following: At step 809, it is determined whether the CD is in spec. If no, the sample frequency is increased at step 810 and the wafers with out-of-spec CD's are rejected at step 811. The rejected wafers are reworked at step 807. The reworking step is referred to very broadly in paragraph [0211] which recites: "the module controller 114 may direct the inventive system 100 to rework the wafer (step 807) as previously described". Rework step 807 was previously described in paragraph [0209], part of which is reproduced above. As provided in paragraph [0209] and as known by one of ordinary skill in the art of semiconductor manufacturing, reworking wafers generally refers to stripping the photoresist then forming another photoresist layer and patterning the same. Sahin discloses no communication with the rework step 807, much less control over this process. Sahin merely dictates that out of spec wafers are sent for rework. Note that the flowchart illustrated in FIG. 8A(1) of Sahin is a flowchart generally showing movement of wafers, not electronic communications. The claimed invention, as in FIG. 3A, includes the rerouting of data related to a product, via software link 44, to the entry point 32 of the photoresist control function 30. Based on this data (see paragraph bridging pages 16-17 of specification), the adjustment sub-system 34 makes a desired determination that provides correction(s) to the controlling data, most notably to the value of ADI CD that must be created and the following paragraph, at lines 7-12 of page 17 indicate that this value is used for the creating of an opening through the layer of photoresist (such that the CD will be within spec limits).

Continuing the examination of Sahin, at step 802, the reworked wafers are received apparently from the lithography tool that is neither illustrated nor discussed in the relevant section of the Sahin specification, i.e., paragraph [0209]. Appellants also

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point out that wafers that are rejected for having an unacceptably high defect density, shown at steps 804 and 806, are sent in the same rework loop to the rework step, step 807. Sahin does not disclose or even suggest that the wafers reworked for completely different reasons – those for high defect density and those for out of spec CD's – are treated any differently at step 807.

Sahin clearly falls short of disclosing the claimed feature of communicating with the means for creating an opening through a layer of etch resist material to control the critical dimension measurement, much less controlling the critical dimension measurement of the opening by implementing corrections and the means for creating an opening through a layer of etch resist material, i.e. the collective lithography tools.

Independent claims 8, 15 and 16 each recite features not disclosed in Sahin and therefore the rejection of claims 8, 15 and 16 under 35 U.S.C. § 102(e) as being anticipated by Sahin, should be reversed. Claims 9-11 each depend from claim 8 and claim 17 depends from claim 16. Claims 9-11 and 17 are similarly distinguished from Sahin by virtue of their respective dependencies. As such, the rejection of claims 9-11 and 17 under 35 U.S.C. § 102(e) as being anticipated by Sahin, should also be reversed.

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**7C. Conclusion.**

In view of the foregoing remarks, Appellants submit that this application is in condition for allowance. Appellants respectfully request that the Board reverse the Examiner's rejection of all pending claims.

Dated: February 18, 2009

Respectfully submitted,



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Attachments: Claims Appendix, Evidence Appendix, Related Proceedings Appendix

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## 8. CLAIMS APPENDIX

### Claims Under Appeal

1   Claims 8-11 and 15-17 are under appeal.

1   8.   A system for creation of an opening of controllable format through a layer of  
2   insulation material, comprising:

3           means for creating an opening through a layer of etch resist material provided  
4   over the surface of a layer of insulating material having been deposited over the surface  
5   of a substrate;

6           means for measuring an obtained critical dimension measurement of said  
7   opening created through said layer of etch resist material;

8           means, including a feedback mechanism, for assuring that the obtained critical  
9   dimension measurement of said opening created through said layer of etch resist  
10   material is within design specification, said feedback mechanism communicating with  
11   said means for creating an opening through a layer of etch resist material to control said  
12   critical dimension measurement of said opening by implementing corrections in said  
13   means for creating an opening through a layer of etch resist material;

14           means for creating an opening through said layer of insulation material, whereby  
15   a diameter of said opening through said layer of insulation material is dependent on a  
16   diameter of said opening created through said layer of etch resist material; and

17           means, including a feedback mechanism, for assuring that said opening created  
18   through said layer of insulation material is within design specification.

1   9.   The system of claim 8, said means, including a feedback mechanism, for  
2   assuring that an obtained critical dimension measurement of said opening created  
3   through said layer of etch resist material is within design specification comprising:

4           means for linking to a software supervisory function, thereby including data  
5   transmission functions;

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6       means for linking to a software function equally being linked to a software  
7       supervisory function, thereby including data transmission functions;  
8       means for data manipulating capabilities, thereby including manipulating  
9       interdependent data;  
10      means for interfacing with semiconductor equipment, thereby including  
11     equipment functioning in a supporting role to said semiconductor equipment; and  
12      means for creating instructions for said semiconductor equipment, thereby  
13     including equipment functioning in a supporting role to said semiconductor equipment.

1       10. The system of claim 8, said means for assuring that said opening created  
2     through said layer of insulation material is within design specification comprising:  
3       means for linking to a software supervisory function, thereby including data  
4     transmission functions;  
5       means for linking to a software function equally being linked to a software  
6     supervisory function, thereby including data transmission functions;  
7       means for data manipulating capabilities, thereby including manipulating  
8     interdependent data;  
9       means for interfacing with semiconductor equipment, thereby including  
10    equipment functioning in a supporting role to said semiconductor equipment; and  
11      means for creating instructions for said semiconductor equipment, thereby  
12     including equipment functioning in a supporting role to said semiconductor equipment.

1       11. The system of claim 8, further comprising means for creating an opening having  
2     non-linear sidewalls through a layer of insulation material by applying a high-polymer  
3     based etch to the surface of said layer of insulation material.

1       15. A system for creation of an opening of controllable format through a layer of  
2     insulation material, comprising:  
3       means for creating an opening through a layer of etch resist material provided  
4     over the surface of a layer of insulating material having been deposited over the surface  
5     of a substrate;

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6 means, including a feedback mechanism, for obtaining a critical dimension  
7 measurement of said opening created through said layer of etch resist material and  
8 assuring that said critical dimension measurement is within design specification, said  
9 feedback mechanism communicating with said means for creating an opening through a  
10 layer of etch resist material to control said critical dimension measurement of said  
11 opening;

12 means for creating an opening having non-linear sidewalls through said layer of  
13 insulation material by applying a high-polymer based etch to the surface of said layer of  
14 insulation material, whereby a diameter of opening having non-linear sidewalls is  
15 dependent on a diameter of said opening created through said layer of etch resist  
16 material; and

17 means, including a feedback mechanism, for assuring that said opening created  
18 through said layer of insulation material is within design specification.

1 16. A system for creation of an opening of controllable format through a layer of  
2 insulation material, comprising:

3 means, including a feedback mechanism, for creating an opening through a layer  
4 of etch resist material provided over the surface of a layer of insulating material having  
5 been deposited over the surface of a substrate, such that the opening has a critical  
6 dimension measurement that is within design specification, said feedback mechanism  
7 communicating with said means for creating an opening through a layer of etch resist  
8 material to control said critical dimension measurement of said opening;

9 means for creating an said opening through said layer of insulation material,  
10 whereby a diameter of said layer of insulation material is dependent on a diameter of  
11 said opening created through said layer of etch resist material; and

12 means, including a feedback mechanism, for assuring that said opening created  
13 through said layer of insulation material is within design specification.

1 17. The system of claim 16, wherein said means, including a feedback mechanism,  
2 for creating an opening, include means for making corrections to an original critical  
3 dimension measurement that is not within design specification.

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**9. EVIDENCE APPENDIX**

Definition of "control", Webster's II New College Dictionary, Houghton Mifflin Co., 1995  
(attached)

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**10. RELATED PROCEEDINGS APPENDIX**

**None**

